23.7 System-in-Silicon Architecture and its Application to H.264/AVC Motion Estimation for 1080HDTV

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The BW between logic and memory is a critical factor in the design of high performance systems. In addition to the conventional approaches, such as DDR/XDR interfaces or embedded DRAM integration, a multi-chip LSI [1], and an embedded wireless communication system [2], have been proposed recently, to achieve higher BW. In this paper, the "System-in-Silicon (SiS)" architecture is proposed to realize the wide BW between logic and relatively large memory with 1.6pJ/b low energy interface. The process, reliability, design methodology, DFT consideration, and the results obtained by the application of this architecture to an H.264/AVC motion estimation system are presented.

Figure 23.7.1 shows the SiS architecture and the cross section SEM of the test chip. Application chips are mounted onto the silicon interposer (SiIP) face-down with 100μm spacing. Each chip is connected to the SiIP by a 50μm pitch eutectic solder bump array. Using this structure, all active devices can be encapsulated into the silicon, and heat at application chips can flow to both top and bottom silicon substrate. The thermal resistance of this structure is estimated to be 10% lower than that of a conventional SoC by 3D thermal simulation.

The SiS assembly starts from mounting application chips onto the SiIP wafer with micro-bumps. Each application chip is a good die sorted before the chip mount. After chip mounting, the SiIP wafer with application chips is processed in a conventional assembly process for dicing and packaging. Through SiS fabrication, the micro-bump formation and the chip mount are implemented in a mature and conventional IC fabrication process. Standard reliability tests are completed to qualify those adopted technologies for SiS using the test chip shown in Fig. 23.7.1. Figure 23.7.2 shows their conditions and the in-situ monitoring charts of the thermal cycle (T/C) and thermal humidity bias (THB) test. Since the coefficient of thermal expansion (CTE) is the same between the daughter and mother chip, a sufficient immunity to T/C stress is obtained as shown in Fig. 23.7.2. The reliability of SiS architecture with the 50μm pitch bumps has been qualified.

Figure 23.7.3 shows the back-end design methodology of the SiS architecture and its routing layer definition. One of the benefits of the SiS architecture is the compatibility with commodity EDA tools, since its architecture corresponds to a block-based or hierarchical SoC design methodology. In the design shown in Fig. 23.7.3, METAL1~6 are assigned to ASIC, and METAL7~8 are assigned to SiIP. The VIA67 is physically the micro-bump, which connects ASIC and SiIP, and it is represented as the via of METAL6 and 7 in the design system. Therefore the design system can handle the entire SiS chip as a monolithic chip including extraction, DRC, LVS, and other physical verifications. After the verification of the entire chip, the photo-mask data of ASIC and SiIP (data should be flipped) are taped out. By using SiS architecture, the chip design can be completed in the SoC design environment with short turn around time, and the best wafer process for each function can be selected and integrated. It means that a pseudo hetero-process integration is realized by the SiS architecture. For instance, high-density DRAM process and generic CMOS logic process are integrated together without any process conflicts. It can be also extended to the integration of other process technologies such as NVM or analog.

Figure 23.7.4 shows the floorplan of the overall concept. An ASIC and two 64Mb specific DRAMs (SiS-DRAM) are integrated onto the SiIP with 57,164 bumps of 50μm pitch. The ASIC is fabricated with a 0.18μm CMOS logic process (TSMC CL018G 1P6M), and SiS-DRAM is fabricated with a 0.11μm commodity DRAM process with triple well and triple layer of metal. The SiIP adopts a 0.5μm double-layer metal technology, which is fine enough to route and mature enough to keep costs low and yield high without a sort. A 1024b wide internal bus is realized by using two SiS-DRAMs, each with a 512b separated data in/outs (D/Qs). All signals of SiS-DRAM are connected to the Interface Macro (IFM) buried in the ASIC as a hard macro. The function of the SiS-DRAM and the connection of micro-bumps can be tested through IFM after SiS assembly. BIST and scan chain test of SiS-DRAM can be controlled from the IFM, and it is possible to analyze fail bits in SiS-DRAM after packaging. The IFM input capacitance for inter-chip connection is reduced to less than 0.3pF/pin by size optimization of buffer and ESD circuitry, and the drivability is also optimized by using internal transistors.

H.264/AVC is the latest video coding standard, which was developed by JVT [3]. A complete encoder chip for 1280×720 video streams has been reported [4] previously. The work presented here is targeted to the motion estimation engine for real-time 1080HDTV (1920×1088) applications, with integrated DRAM using the SiS architecture. Figure 23.7.5 shows the system architecture and the chip features. Data for the current frame and the reference picture are stored in SiS-DRAM. Via IFM, the current macro-block (MB) is transferred to a register file, and the reference picture is transferred to an SRAM. Then they are scheduled by the PE-Scheduler into 16 PEs for a sum of absolute differences (SAD) and cost calculation. SAD and cost results decide a final block mode and motion vectors. The SiS-DRAM works at 25MHz to reduce the power consumption, however, the motion estimation core works at 200MHz to increase the processing capability. Combining the pipeline scheme and the parallelism, only 760 clock cycles are needed to process one MB, therefore the chip achieves 263.1K Macro Blocks per second (MB/s) for 1080HDTV processing. To realize this performance, a minimum BW of 23.1Gb/s is required for frame memory bus transactions.

Figure 23.7.6 shows a comparison of 23.1Gb/s BW realizations. This work achieves it with a frequency of 25MHz and a 1024b wide bus. Furthermore, the power consumption for the data transaction between ASIC and SiS-DRAMs is only 37mW including IMF power. Therefore, this yields a data transfer energy efficiency of 1.6pJ/b. This approach is quite different from a high frequency off-chip solution with terminators, and can be very efficient especially in mobile applications.

Figure 23.7.7 shows the micrographs of the SiIP, the ASIC, and the SiS-DRAMs. In its assembled form the ASIC chip and two SiS-DRAM chips are flipped and mounted on a SiIP die.

References:

[1] T. Ezaki et. al., "A 160Gb/s Interface Design Configuration for Multichip LSI," *ISSCC Dig. Tech. Papers*, pp. 140-141, Feb., 2004

[2] N. Miura et. al., "A 195Gb/s 1.2W 3D-Starcked Inductive Inter-Chip Wireless Superconnect with Transmit Power Control Scheme," *ISSCC Dig. Tech. Papers,* pp. 264-265, Feb., 2005

[3] Joint Video Team of ISO/IEC MPEG & ITU-T VCEG, "Draft ITU-T Recommendation H.264 and Final Draft International Standard 14496-10 Advanced Video Coding," ISO/IEC JTC1/SC29/WG11 and ITU-T SG16/Q.6, May, 2003.

[4] Yu-Wen Huang, Tung-Chien, et al., "A 1.3TOPS H.264/AVC Single Chip Encoder for HDTV Applications," *ISSCC Dig. Tech. Papers*, pp. 128-129, Feb., 2005.

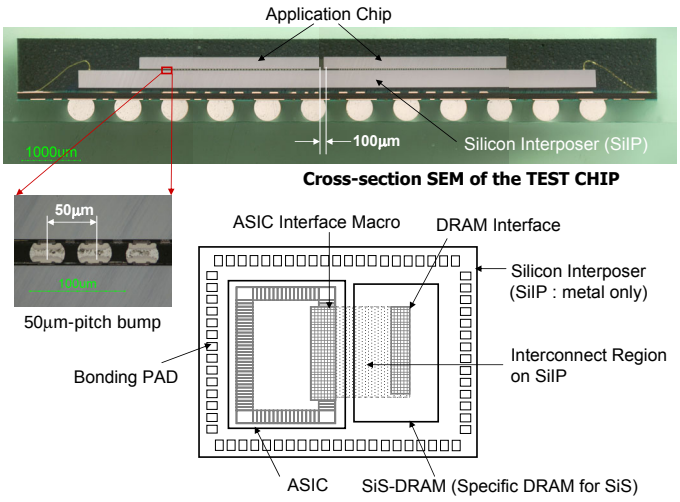


Figure 23.7.1: System-in-Silicon Architecture.

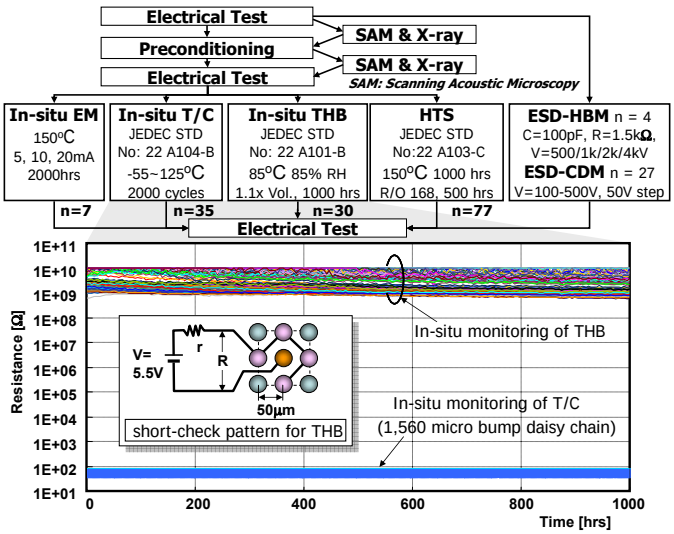


Figure 23.7.2: Reliability of System-in-Silicon.

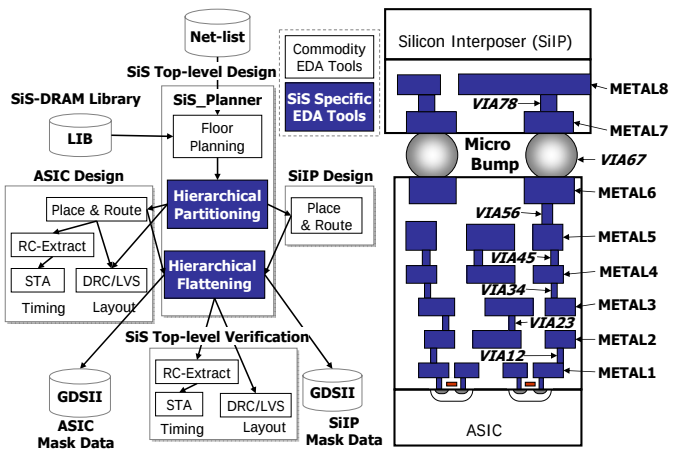


Figure 23.7.3: Design Flow and Layer Definition.

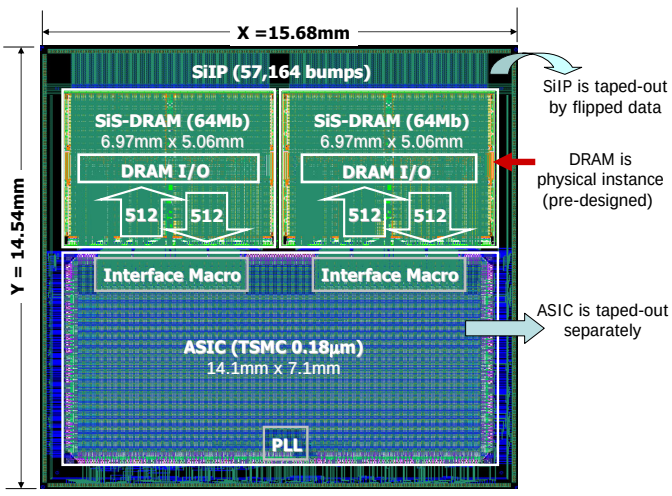
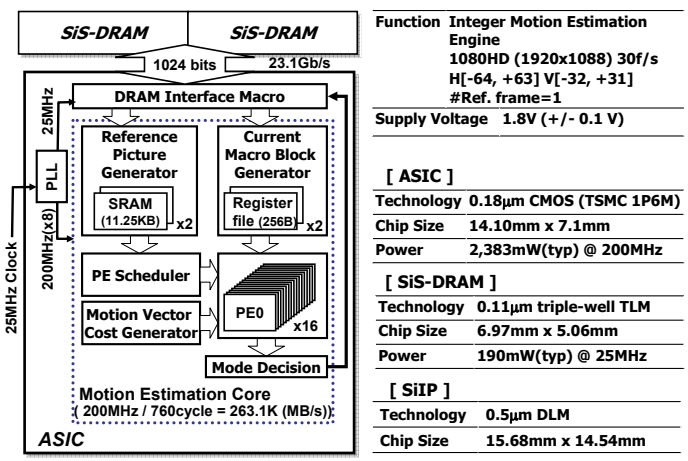


Figure 23.7.4: Chip Layout and Interface Macro.



Function	Integer Motion Estimation Engine 1080HD (1920x1088) 30f/s H[-64, +63] V[-32, +31] #Ref. frame=1
Supply Voltage	1.8V (+/- 0.1 V)

[ASIC]	
Technology	0.18μm CMOS (TSMC 1P6M)
Chip Size	14.10mm x 7.1mm
Power	2,383mW(typ) @ 200MHz

[SiS-DRAM]	
Technology	0.11μm triple-well TLM
Chip Size	6.97mm x 5.06mm
Power	190mW(typ) @ 25MHz

[SiIP]	
Technology	0.5μm DLM
Chip Size	15.68mm x 14.54mm

Figure 23.7.5: Architecture and Features of the Chip.

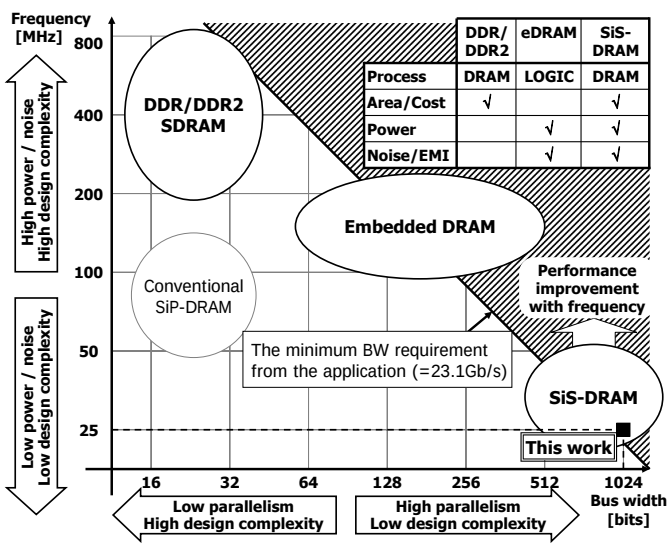


Figure 23.7.6: Comparison of 23.1Gb/s BW Realization.

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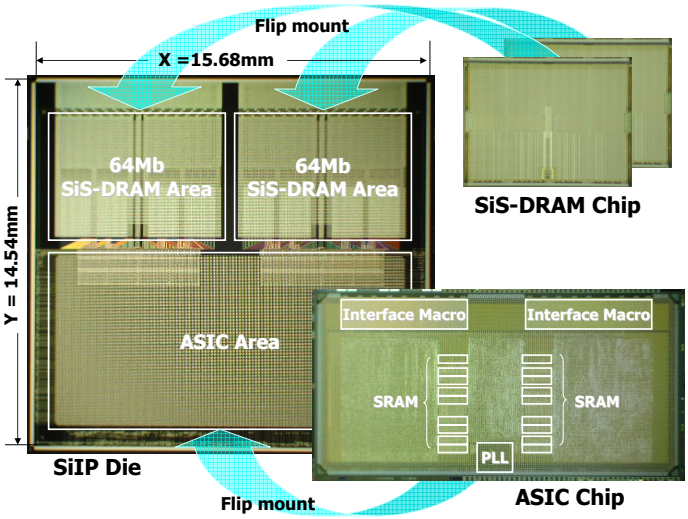

Figure 23.7.7: Micrographs.

